Application No. 09/836,777
Filed: April 17, 2001
TC Art Unit: 2664
Confirmation No.: 6860

REMARKS

The foregoing amendment is filed in response to the official action dated August 19, 2005. Reconsideration is respectfully requested.

The status of the claims is as follows:

Claims 1-12 are currently pending.

Claims 1-4, 6-8, and 10-12 stand rejected.

Claims 5 and 9 are objected to.

Claims 1, 7, and 11 have been amended.

The Examiner has rejected claims 1-4, 6-8, and 10-12 under 35 U.S.C. 102(e) as being anticipated by Diaconescu *et al.* (USP 6,738,395). The Applicant respectfully submits, however, that the Diaconescu reference does not disclose each and every element/step of base claims 1, 7, and 11. Notwithstanding the failure of the Diaconescu reference to disclose each and every element/step of base claims 1, 7, and 11, the Applicant has amended base claims 1, 7, and 11 to more definitively recite the subject matter claimed therein. It is respectfully submitted that the rejections of base claims 1, 7, and 11, as amended, and the claims dependent therefrom, under section 102 of the Patent Laws are unwarranted and should be withdrawn.



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For example, the cited Diaconescu reference does not disclose the SONET multiplexed communications system of amended claim 1, which recites at least one SONET input signal path for receiving at least one input signal, the SONET input signal path including a pointer interpreter for interpreting at least one input signal pointer, at least one SONET output signal path for transmitting at least one output signal corresponding to the input signal, the SONET output signal path including a pointer generator for generating at least one output signal pointer, and a time slot interchange circuit operatively coupled *between* the pointer interpreter and the pointer generator included in the SONET input and output signal paths, respectively, the time slot interchange circuit being configured to provide time division multiplexed connections for the input and output signals, in which the SONET input signal path further includes a synchronization buffer serially coupled to the pointer interpreter, the synchronization buffer for transferring the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit, and in which the SONET output signal path further includes a first-in first-out buffer serially coupled to the pointer generator, the first-in first-out buffer for transferring the output signal from the respective clock rate



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of the time slot interchange circuit to a respective clock rate of the SONET output signal path. The SONET multiplexed communications system of amended claim 1 is described throughout the instant application, for example, see page 11, lines 3-27, and Fig. 2a, of the application.

Instead of disclosing a SONET multiplexed communications system that includes a time slot interchange circuit operatively coupled between a pointer interpreter and a pointer generator included in a SONET input signal path and a SONET output signal path, respectively, as recited in amended claim 1, Diaconescu *et al.* disclose a system for performing pointer processing that includes a plurality of conventional pointer processor blocks, specifically, a parallel array of N pointer processing strips or SYNC blocks **14**, a data distribution or first time slot interchange (TSI) block **16**, and a data collection or second time slot interchange (TSI) block **20** (see column 5, line 63, to column 6, line 40, and Fig. 3, of Diaconescu *et al.*). As disclosed in the Diaconescu reference, each of the SYNC blocks **14** includes a pointer interpreter, an elastic store, and a pointer generator, like the conventional pointer processor block depicted in Fig. 1 of Diaconescu *et al.* (see also column 6, lines 17-20, of Diaconescu *et al.*).



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The Applicant respectfully submits that the system for performing pointer processing disclosed by Diaconescu *et al.* does not anticipate the SONET multiplexed communications system of claim 1. As recited in amended claim 1, the SONET multiplexed communications system includes a time slot interchange circuit operatively coupled between a pointer interpreter and a pointer generator included in a SONET input signal path and a SONET output signal path, respectively. In contrast, as disclosed in the Diaconescu reference, the system for performing pointer processing includes two TSI blocks **16** and **20**, neither of which is operatively coupled between a pointer interpreter and a pointer generator, as recited in amended claim 1.

As explained above, each of the SYNC blocks **14** (see Fig. 3 of Diaconescu *et al.*) includes a pointer interpreter, a pointer generator, and an elastic store disposed between the pointer interpreter and the pointer generator. The Applicant points out that the TSI block **16** is coupled at the inputs of the pointer interpreters contained in the SYNC blocks #1 and #N **14**, and that the TSI block **20** is coupled at the outputs of the pointer generators contained in the SYNC blocks #1 through #N **14** (see Fig. 3 of Diaconescu *et al.*). Significantly, neither one of the TSI blocks **16** and **20** of the Diaconescu reference is operatively



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coupled *between* the pointer interpreter and the pointer generator included in any one of the SYNC blocks **14**. The system of amended claim 1, which includes a time slot interchange circuit operatively coupled between a pointer interpreter and a pointer generator included in a SONET input signal path and a SONET output signal path, respectively, therefore clearly distinguishes over the system disclosed by Diaconescu *et al*.

In addition, the cited Diaconescu reference does not disclose the SONET multiplexed communications system of amended claim 7, which includes at least one SONET input signal path for receiving at least one input signal, the SONET input signal path including a synchronization buffer, at least one SONET output signal path for transmitting at least one output signal corresponding to the input signal, the SONET output signal path including a pointer interpreter for interpreting at least one input signal pointer, a pointer generator for generating at least one output signal pointer, and a first-in first-out buffer serially coupled between the pointer interpreter and the pointer generator, and at least one time slot interchange circuit operatively coupled *between* the synchronization buffer and the pointer interpreter included in the SONET input and output signal paths, respectively, the time slot interchange circuit for providing time division multiplexed



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connections for the input and output signals, in which the synchronization buffer included in the SONET input signal path is configured to transfer the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit, and in which the first-in first-out buffer included in the SONET output signal path is configured to transfer the output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path. The SONET multiplexed communications system of amended claim 7 is described throughout the instant application, for example, see page 26, line 13, to page 27, line 3, of the application.

Instead of disclosing a SONET multiplexed communications system that includes a time slot interchange circuit operatively coupled between a synchronization buffer and a pointer interpreter included in a SONET input signal path and a SONET output signal path, respectively, as recited in amended claim 7, Diaconescu *et al.* disclose the system for performing pointer processing including the conventional pointer processor blocks, *i.e.*, the SYNC blocks **14**, the first TSI block **16**, the second TSI block **20**, and a delay block **18**, which controls data processing on at least



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two of the pointer processing strips **14** (see column 6, lines 46-49, and Fig. 3, of Diaconescu *et al.*).

The Applicant respectfully submits that the system for performing pointer processing disclosed by Diaconescu *et al.* does not anticipate the SONET multiplexed communications system of claim 7. As recited in amended claim 7, the SONET multiplexed communications system includes a time slot interchange circuit operatively coupled between a synchronization buffer and a pointer interpreter included in a SONET input signal path and a SONET output signal path, respectively. In contrast, as disclosed in the Diaconescu reference, the system for performing pointer processing includes the two TSI blocks **16** and **20**, neither of which is operatively coupled between a synchronization buffer and a pointer interpreter, as recited in amended claim 7. Instead, the TSI block **16** is coupled at the inputs of the pointer interpreters contained in the SYNC blocks #1 and #N **14** and at the input of the delay block **18**. Further, the TSI block **20** is coupled at the outputs of the pointer generators contained in the SYNC blocks #1 through #N **14** (see Fig. 3 of Diaconescu *et al.*). Significantly, neither one of the TSI blocks **16** and **20** of the Diaconescu reference is operatively coupled between a synchronization buffer and a pointer interpreter. The system of amended claim 7, which



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includes a time slot interchange circuit operatively coupled between a synchronization buffer and a pointer interpreter included in a SONET input signal path and a SONET output signal path, respectively, therefore clearly distinguishes over the system disclosed by Diaconescu *et al*.

In addition, the cited Diaconescu reference does not disclose the method of operating a SONET multiplexed communications system of amended claim 11, which includes providing at least one SONET input signal path including a pointer interpreter and a synchronization buffer serially coupled to the pointer interpreter, providing at least one SONET output signal path including a pointer generator and a first-in first-out buffer serially coupled to the pointer generator, providing a time slot interchange circuit operatively coupled *between* the pointer interpreter and the pointer generator included in the SONET input and output signal paths, respectively, receiving at least one input signal by the SONET input signal path, interpreting at least one input signal pointer by the pointer interpreter included in the SONET input signal path, transferring the input signal from a respective clock rate of the SONET input signal path to a respective clock rate of the time slot interchange circuit by the synchronization buffer included in the SONET input signal path,



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providing time division multiplexed connections for the input signal and at least one corresponding output signal by the time slot interchange circuit, generating at least one output signal pointer by the pointer generator included in the SONET output signal path, transferring the corresponding output signal from the respective clock rate of the time slot interchange circuit to a respective clock rate of the SONET output signal path by the first-in first-out buffer included in the SONET output signal path, and transmitting the corresponding output signal by the SONET output signal path. The method of operating a SONET multiplexed communications system of amended claim 11 is described throughout the instant application, for example, see page 11, lines 3-27, and Fig. 2a, of the application.

As explained above with reference to amended claim 1, instead of disclosing a SONET multiplexed communications system that includes a time slot interchange circuit operatively coupled between a pointer interpreter and a pointer generator included in a SONET input signal path and a SONET output signal path, respectively, Diaconescu *et al.* disclose the system for performing pointer processing that includes the two TSI blocks **16** and **20**, neither of which is operatively coupled between a pointer interpreter and a pointer generator, as recited in amended claim



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11. The method of amended claim 11, which includes the step of providing a time slot interchange circuit operatively coupled between a pointer interpreter and a pointer generator included in a SONET input signal path and a SONET output signal path, respectively, therefore clearly distinguishes over the disclosure of Diaconescu *et al.*

Important advantages are achieved by providing the systems of amended base claims 1 and 7, and the method of amended base claim 11. For example, the claimed systems and method permit greater integration when the time slot interchanger has more inputs than outputs, and/or the time slot interchanger provides each SONET output signal to a pointer processor included in an appropriate SONET output signal path to transfer the SONET output signal to the clock rate of the SONET output signal path (see page 4, lines 24-30, of the application). None of the cited references, including the Diaconescu reference, teaches or suggests such important advantages.

Because, as explained above, the subject matter of each of amended base claims 1, 7, and 11 distinguishes over the disclosure of Diaconescu *et al.*, the Applicant respectfully submits that the Diaconescu reference does not anticipate amended claims 1, 7, and 11 and the claims dependent therefrom. Accordingly, it is



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respectfully submitted that the rejections of claims 1-4, 6-8, and 10-12 under 35 U.S.C. 102 are unwarranted and should be withdrawn.

The Applicant points out that claims 5 and 9 were rewritten in independent form as suggested in the official action, including all of the limitations of the base claim and any intervening claims, in the Applicant's prior response dated February 25, 2005. Accordingly, it is respectfully submitted that claims 5 and 9, as presented in the foregoing amendment, should be allowed.

In view of the foregoing, it is respectfully submitted that the present application is in a condition for allowance. Early and favorable action is respectfully requested.

The Examiner is encouraged to telephone the undersigned Attorney to discuss any matter that would expedite allowance of



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Application No. 09/836,777
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the present application.

Respectfully submitted,

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Enclosure



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